	Type	L #	Hits	Search Text	DBs	Time Stamp
1	IS&R	L2	2	("6391742").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/31 18:54
2	BRS	L3	5	("5798557" | "5901031" | "6036872" | "6146917" | "6232150").PN.	USPAT	2004/10/31 18:25
3	BRS	L4	5	("5798557" | "5901031" | "6036872" | "6146917" | "6232150").PN.	USPAT	2004/10/31 18:27
4	BRS	L5	9	6391742.URPN.	USPAT	2004/10/31 18:27
5	BRS	L6	5	("5798557" | "5901031" | "6036872" | "6146917" | "6232150").PN.	USPAT	2004/10/31 18:28
6	BRS	L7	2991581	(via near hole) or (through near hole) or opening	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/31 18:37
7	BRS	L8	957235	bump or solder$6 or ball	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/31 18:37
8	BRS	L9	524301	pad	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/31 18:38

	Type	L #	Hits	Search Text	DBs	Time Stamp
9	BRS	L10	100300	"glass substrate"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/31 18:38
10	BRS	L11	3820	7 near8 8 near8 9	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/31 18:38
11	BRS	L12	23743	"flip chip"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/31 18:39
12	BRS	L13	9	11 same 10	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/31 18:40
13	BRS	L14	114	11 and 10	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/31 18:40

	Type	L #	Hits	Search Text	DBs	Time Stamp
14	BRS	L15	45	14 and 12	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/31 18:41
15	BRS	L16	23383199	(@ad<20030224) or (@rlad<20030224)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/31 18:41
16	BRS	L17	41	15 and 16	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/31 18:41
17	BRS	L18	19	("5407864" | "5422516" | "5468681" | "5495667" | "5569963" | "5604160" | "5734201" | "5790384" | "5798557" | "5821624" | "5847456" | "5851845" | "5886409" | "5972734" | "6004867" | "6037665" | "6081026" | "6081429" | "6097098").PN.	USPAT	2004/10/31 18:51
18	IS&R	L19	2709	(438/106).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/31 18:54

	Type	L #	Hits	Search Text	DBs	Time Stamp
19	IS&R	L23	812	(438/125).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/31 19:09
20	IS&R	L21	823	(438/455).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/31 19:34
21	IS&R	L24	193	(438/456).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/31 19:40

US-PAT-NO: 6413799

DOCUMENT-IDENTIFIER: US 6413799 B1

TITLE: Method of forming a ball-grid array package at a wafer level

---------- KWIC ---------

Abstract Text - ABTX (1):

A method of forming an integrated circuit at the wafer level. The integrated circuit package occupies a minimum amount of space on an end-use printed circuit board. A pre-fabricated interposer substrate, made of metal circuitry and a dielectric base, has a plurality of metallized openings which are aligned with metallized wirebond pads on the top surface of a silicon wafer. Solder, or conductive adhesive, is deposited through the metallized openings to form the electrical connection between the circuitry on the interposer layer and the circuitry on the wafer. **Solder balls are then placed on the metal pad openings** on the interposer substrate and are reflowed to form a wafer-level BGA structure. The wafer-level BGA structure is then cut into individual BGA chip packages.

Application Filing Date - AD (1):

20000725

Brief Summary Text - BSTX (12):

The above objects have been achieved in a method of forming an integrated circuit package on the wafer level using a **flip chip** design with a single wafer. The integrated circuit package is formed by first

providing a product
silicon wafer having a plurality of microelectric circuits fabricated thereon
and having a plurality of standard aluminum bonding pads exposed. The aluminum
bonding pads are re-metallized to be solderable. Then, a layer of adhesive is
deposited onto the wafer surface, the bonding pads remaining exposed. A
pre-fabricated interposer substrate, having metallized openings, is aligned to
the wafer and then the assembly is cured. Solder, or conductive adhesive, is
then deposited through the openings in the substrate and the assembly is
reflowed, or cured, to form the electrical connection between the circuitry on
the substrate and the bonding pads on the silicon wafer. Solder balls are then
placed on the metal pads on the substrate and are then reflowed forming a BGA
structure. The wafer is then diced and the individual BGA packages are formed.
The BGA package is flipped for mounting on a circuit board.

Detailed Description Text - DETX (5):
With reference to FIG. 5, an interposer substrate layer 30 is then secured
on top of the elastomer layer 27 to form a wafer assembly 39. The interposer
substrate 30 is a preformed substrate consisting of metal circuitry 34 and a
dielectric base 32. The metal circuitry 34 typically consists of copper traces
formed throughout the substrate. The interposer substrate 30 can also include
solder resist coatings to help define solder wetable areas on the copper metal
circuitry. The metal circuitry 34 can be formed on a single layer or on
multiple layers of the interposer substrate 30. The copper metal circuitry can
be nickel-gold plated or coated by an organic material. The dielectric base
material 32 is typically made of a polyamide base substrate. Alternatively, BT
resin and other epoxy-**glass substrates** can also be used as

the dielectric base material 32. The metal circuitry 34 generally serves as interconnect circuitry, as the traces can be routed throughout the substrate to interconnect the circuits from the various bonding pads 23 to the Input/Output (I/O) interconnects which will be added to the wafer assembly 39, as described later with reference to FIG. 7.

Related Application Filing Date - RLFD (1):
19991214